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				Application Number	TBD
				Filing Date	Herewith
				First Named Inventor	Ting, <i>et al.</i>
				Art Unit	TBD
				Examiner Name	TBD
Sheet	1	of	1	Attorney Docket Number	TSM03-0945

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No.	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code ² (if known)			
SWC		US-2003/0067045 A1	04-10-2003	Sugiyama et al.	
		US-			
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FOREIGN PATENT DOCUMENTS						
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NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
SWC		GHANI, T. <i>et al.</i> , "100 nm Gate Length High Performance/Low Power CMOS Transistor Structure," IEDM (1999) pp. 415-418.	
SWC		NAKAI, S., <i>et al.</i> , "A 100 nm CMOS Technology with "Sidewall-Notched" 40 nm Transistors and SiC-Capped Cu/VLK Interconnects for High Performance Microprocessor Applications," 2002 Symposium on VLSI Technology Digest of Technical Papers (2002) pp. 66-67.	
SWC		PIDIN, S., <i>et al.</i> , "Experimental and Simulation Study on Sub-50 nm CMOS Design," 2001 Symposium on VLSI Technology Digest of Technical Papers (2001) pp. 35-36.	

Examiner Signature	CRANE	Date Considered	11/2005
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